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EXAMINER	
CLEARY, THOMAS J	
ART UNIT	**PAPER NUMBER**
2111	

DATE MAILED: 04/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/056,631	WORRELL, FRANK	
	Examiner	Art Unit	
	Thomas J. Cleary	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 13, and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent Number 4,853,847 to Ohuchi ("Ohuchi").

3. In reference to Claim 1, Ohuchi discloses a bus comprising: a master interface configured to (i) receive an early command signal having a predetermined timing relationship to a first clock edge (See Figure 5 'WRRQ') and (ii) present a bus wait signal proximate a second clock edge (See Figure 5 'WAIT'); a slave interface configured to (i) present a command signal a delay after said first clock edge (See Figure 5 'WRRQIO') and (ii) receive a slave wait signal (See Figure 5 'WAITI'); and a control logic configured to (i) register said early command signal to generate said command signal (See Figures 2 and 3 Number 38 and Column 3 Lines 35-53) and (ii) convert said slave wait signal into said bus wait signal (See Figures 2 and 3 Number 38 and Column 3 Lines 56-61).

4. Claims 13 and 20 recite limitations which are substantially equivalent to the limitations of Claim 1, and thus are rejected under similar reasoning as applied in the rejection of Claim 1 above.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 2, 8, 9, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohuchi as applied to Claims 1 and 13 above, and further in view of US Patent Number 5,291,080 to Amagasaki ("Amagasaki").

7. In reference to Claim 2, Ohuchi teaches the limitations as applied to Claim 1 above. Ohuchi further teaches that said master interface is further configured to receive an early address signal having said predetermined timing relationship with said first clock edge (See Figure 2 Number 16), said control logic is further configured to register said early address signal to generate an address signal (See Figure 2 Number 44, Figure 5 'AREG', and Column 4 Lines 37-42), and said slave interface is further

configured to present said address signal said delay after said first clock edge (See Figure 5 'AREG'). Ohuchi does not teach that said control logic is further configured to decode said address signal to generate a device select signal and said slave interface is further configured to present said device select signal said delay after said first clock edge. Amagasaki teaches a control unit receiving an address signal, decoding said address signal to produce a device select signal, and presenting said device select signal to the selected device (See Abstract, Figure 1 Number 3, and Column 1 Line 60 – Column 2 Line 3).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Ohuchi with the address decoding and device select signal generation of Amagasaki, resulting in the invention of Claim 2, in order to reduce power consumption by only providing data to the internal device to which it is directed (See Column 1 Lines 7-51 of Amagasaki).

8. In reference to Claim 8, Ohuchi teaches the limitations as applied to Claim 1 above. Ohuchi does not teach that said control logic comprises an address decoder configured to generate a plurality of device select signals responsive to an address signal. Amagasaki teaches a control unit receiving an address signal and decoding said address signal to produce a plurality of device select signals (See Abstract, Figure 1 Number 3, and Column 1 Line 60 – Column 2 Line 3).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Ohuchi with the address decoding and

device select signal generation of Amagasaki, resulting in the invention of Claim 8, in order to reduce power consumption by only providing data to the internal device to which it is directed (See Column 1 Lines 7-51 of Amagasaki).

9. In reference to Claim 9, Ohuchi and Amagasaki teach the limitations as applied to Claim 8 above. Ohuchi further teaches that the control logic further comprises a plurality of registers (See Figure 3 Numbers 42 and 44) configured to register a plurality of early signals each having said predetermined relationship to said first clock edge to generate a plurality of signals said delay after said first clock edge (See Figure 5 'AREG' and 'DWREG' and Column 4 Lines 37-42).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Ohuchi with the address decoding and device select signal generation of Amagasaki, resulting in the invention of Claim 9, in order to reduce power consumption by only providing data to the internal device to which it is directed (See Column 1 Lines 7-51 of Amagasaki).

10. Claim 14 recites limitations which are substantially equivalent to the limitations of Claim 2, and thus is rejected under similar reasoning as applied in the rejection of Claim 2 above.

11. Claims 3 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohuchi and Amagasaki as applied to Claims 2 and 14 above, and further in view of US Patent Number 5,412,662 to Honma et al. ("Honma").

12. In reference to Claim 3, Ohuchi and Amagasaki teach the limitations as applied to Claim 2 above. Ohuchi and Amagasaki do not teach that said master interface is further configured to receive a no-address signal having said predetermined relationship to said first clock signal and said control logic is further configured to inhibit said slave select signal in response to said no-address signal. Honma teaches receiving a signal, which is equivalent to a no-address signal, that is used by control logic to inhibit a select signal (See Figure 5 Number 3A and Column 6 Lines 35-41).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Ohuchi and Amagasaki with the select signal inhibit signal of Honma, resulting in the invention of Claim 3, in order to prevent an overwrite of the data written to the currently selected device (See Column 6 Lines 48-62 of Honma).

13. Claim 15 recites limitations which are substantially equivalent to the limitations of Claim 3, and thus is rejected under similar reasoning as applied in the rejection of Claim 3 above.

14. Claims 4 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohuchi as applied to Claims 1 and 13 above, and further in view of US Patent Number 6,085,261 to McIntyre, Jr. et al. ("McIntyre").

15. In reference to Claim 4, Ohuchi teaches the limitations as applied to Claim 1 above. Ohuchi does not teach that said master interface is further configured to receive an early burst request signal having said predetermined timing relationship to said first clock edge, said control logic is further configured to register said early burst request signal to generate a burst request signal, and said slave interface is further configured to present said burst request signal said delay after said first clock edge. McIntyre teaches a master device (See Figure 1 Number 5) that sends a burst request signal (See Figure 2 Number 27) to a control device (See Figure 1 Number 4), which then sends a burst request signal (See Figure 3 Number 26) to a slave device (See Column 3 Lines 9-33).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Ohuchi with the burst request scheme of McIntyre, resulting in the invention of Claim 4, in order to efficiently enhance the performance of a data processing system by reducing access time by allowing multiple transfers in response to a single address prompt (See Column 1 Lines 31-40 of McIntyre).

16. Claim 16 recites limitations which are substantially equivalent to the limitations of Claim 4, and thus is rejected under similar reasoning as applied in the rejection of Claim 4 above.

17. Claims 5, 6, 17, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohuchi as applied to Claims 1 and 13 above, and further in view of US Patent Application Publication Number 2001/0010063 to Hirose et al. ("Hirose").

18. In reference to Claim 5, Ohuchi teaches the limitations as applied to Claim 1 above. Ohuchi does not teach that said master interface is further configured to receive a bus request signal and present a bus grant signal, and said control logic is further configured to arbitrate in response to said bus request signal and generate said bus grant signal. Hirose teaches sending a bus request signal to an arbitrator which then generates a bus grant signal (See Page 4 Paragraph 67).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Ohuchi with the bus arbitration scheme of Hirose, resulting in the invention of Claim 5, in order to control the access right to the bus (See Page 4 Paragraphs 65-66 of Hirose).

19. In reference to Claim 6, Ohuchi and Hirose teach the limitations as applied to Claim 5 above. Hirose further teaches completing the arbitration within one clock cycle

and presenting the command signal in the next clock cycle (See Figure 5B and Page 4 Paragraph 65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Ohuchi with the bus arbitration scheme of Hirose, resulting in the invention of Claim 6, in order to control the access right to the bus (See Page 4 Paragraphs 65-66 of Hirose).

20. Claim 17 recites limitations which are substantially equivalent to the limitations of Claim 5, and thus is rejected under similar reasoning as applied in the rejection of Claim 5 above.

21. Claim 18 recites limitations which are substantially equivalent to the limitations of Claim 6, and thus is rejected under similar reasoning as applied in the rejection of Claim 6 above.

22. Claims 7 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohuchi and Hirose as applied to Claim 5 above, and further in view of US Patent Number 6,282,583 to Pincus et al. ("Pincus").

23. In reference to Claim 7, Ohuchi and Hirose teach the limitations as applied to Claim 5 above. Ohuchi and Hirose do not teach that said master interface is further configured to receive a lock signal and said control logic is further configured to halt

arbitration responsive to said lock signal. Pincus teaches a master interface sending a lock signal (See Column 24 Lines 9-19) to a control logic (See Figure 13A), which then halts arbitration in response to said control logic (See Column 24 Lines 24-26).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Ohuchi and Hirose with the lock signal and arbitration halting of Pincus, resulting in the invention of Claim 7, in order to provide indivisible read-modify-write sequences of memory (See Column 12 Line 66 – Column 13 Line 1 of Pincus).

24. Claim 19 recites limitations which are substantially equivalent to the limitations of Claim 7, and thus is rejected under similar reasoning as applied in the rejection of Claim 7 above.

25. Claims 10, 11, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohuchi and Amagasaki as applied to Claim 9 above, and further in view of US Patent Number 5,432,907 to Picazo, Jr. et al. ("Picazo").

26. In reference to Claim 10, Ohuchi and Amagasaki teach the limitations as applied to Claim 9 above. Ohuchi and Amagasaki do not teach that said control logic further comprises an arbitration logic configured to generate a bus grant signal. Picazo teaches a control logic that has bus arbitration logic configured to generate a bus grant signal (See Figure 6B Number 610 and Column 30 Lines 42-55).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Ohuchi and Amagasaki with the bus arbitration logic of Picazo, resulting in the invention of Claim 10, in order to arbitrate requests for access to the data, address, and control buses such that the memory may be shared between the requesting devices (See Column 30 Lines 48-53 of Picazo).

27. In reference to Claim 11, Ohuchi, Amagasaki, and Picazo teach the limitations as applied to Claim 10 above. Picazo further teaches that the control logic comprises a multiplexer configured to multiplex control signals, which are equivalent to the early signals, responsive to the bus grant signal (See Figure 6B Numbers 610, 632, 604, 608, 660, 622, and 637 and Column 31 Lines 32-36).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Ohuchi and Amagasaki with the bus arbitration logic and multiplexer of Picazo, resulting in the invention of Claim 11, in order to arbitrate requests for access to the data, address, and control buses such that the memory may be shared between the requesting devices (See Column 30 Lines 48-53 and Column 31 Lines 35-36 of Picazo).

28. In reference to Claim 12, Ohuchi, Amagasaki, and Picazo teach the limitations as applied to Claim 11 above. Picazo further teaches a second multiplexer that selects a write control signal based on the bus grant signal (See Figure 6B Numbers 610 and 640 and Column 31 Lines 25-31).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Ohuchi and Amagasaki with the bus arbitration logic and multiplexers of Picazo, resulting in the invention of Claim 12, in order to arbitrate requests for access to the data, address, and control buses such that the memory may be shared between the requesting devices (See Column 30 Lines 48-53 and Column 31 Lines 35-36 of Picazo) and to allow the devices to be either written or read by the microprocessors (See Column 31 Lines 27-31 of Picazo).

Response to Arguments

29. Applicant's arguments filed 20 December 2004 have been fully considered but they are not persuasive.

30. Applicant has argued that Ohuchi does not disclose a predetermined timing relationship between signal WRRQ and an edge of signal CLK (See Page 11 Paragraph 1). In response, the Examiner notes that the claim does not define what a "predefined relationship" is. Absent further claim limitations defining the relationship between WRRQ and CLK, any relationship between the signals is a predefined relationship within the scope of the claims.

31. Applicant has argued that Ohuchi does not present signal WRRQIO at the slave interface (See Page 11 Paragraph 2). In response, the Examiner notes that the claim

does not require the signal to be presented to the bus and does not prohibit the signal being presented elsewhere, including another portion of the slave interface, by the slave interface.

32. Applicant has argued that Ohuchi does not present signal WRRQIO a delay after the first clock edge (See Page 11 Paragraph 3). In response, the Examiner notes that the claim does not define what the delay is. As shown in Figure 5, WRRQIO is presented after the first clock edge, and as such, there is inherently a delay. Further, Figure 4 shows that WRRQIO is dependent upon the output of gate 54, which has an inverted clock signal as an input, and thus WRRQIO is not set independently of CLK.

33. Applicant has argued that Ohuchi does not present signal WAITI at the slave interface (See Page 12 Paragraph 1). In response, the Examiner notes that the claim does not require the signal to be presented to the bus and does not prohibit the signal being presented elsewhere, including another portion of the slave interface, by the slave interface. Further, the claim only requires that the slave wait signal be received at the slave interface, not that it be presented at the slave interface. Still further, the claim does not require the signal to be received from the bus and does not prohibit the signal from being received from elsewhere, including another portion of the slave interface.

34. Applicant has argued that the control logic of Ohuchi is a part of the slave processor and not a part of the bus (See Page 12 Paragraph 2). In response, the

Examiner notes that the claim does not prohibit the control logic from being part of the slave interface. Further, since the slave interface is a part of the bus, and the control logic is a part of the slave interface, the control logic is inherently a part of the bus.

35. Applicant has argued that Ohuchi does not suggest control logic configured to convert a slave wait signal into a master wait signal (See Page 12 Paragraph 3). In response, the Examiner notes that gates 58 and 60 of Figure 4 are used to convert the signal WAITI into the signal WAIT, which Applicant has acknowledged is asserted similar to the claimed bus wait signal.

36. In response to Applicant's argument that Ohuchi, Honma, and Pincus are nonanalogous art (See Page 14 Paragraph 3), it has been held that a prior art reference must either be in the field of Applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the Applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, Ohuchi is directed towards performing reads and writes of another device, Honma is directed towards a system capable of enabling and disabling signals to a selected device, and Pincus is directed towards communicating between a plurality of devices. When constructing the device of Ohuchi, one of ordinary skill in the art would naturally look to various methods of communications, such as those taught by Honma and Pincus. Applicant has further argued that the art is non-analogous due to their different classifications. In response,

the Examiner notes that the classification is based on what a patent claims, and not necessarily what it discloses. As such, patents disclosing related material can be classified differently.

37. Applicant has argued that Ohuchi does not teach a relationship between a signal ASSRESS and a signal CLK (See Page 15 Paragraph 2). In response, the Examiner notes that the claim does not define what a "predefined timing relationship" is. Absent further claim limitations defining the relationship between ADDRESS and CLK, any relationship between the signals is a predefined relationship within the scope of the claims.

38. Applicant has argued that Ohuchi does not present signal AREG at the slave interface of the system bus nor having a delay after a first clock edge of the signal CLK (See Page 15 Paragraph 3). In response, the Examiner notes that the claim does not require the signal to be presented to the bus and does not prohibit the signal being presented elsewhere, including another portion of the slave interface, by the slave interface. Further, the Examiner notes that the claim does not define what the delay is. As shown in Figure 5, AREG is presented after the first clock edge, and as such, there is inherently a delay.

39. Applicant has argued that Ohuchi does not teach a predetermined timing relationship between the early signals and the signal CLK (See Page 16 Paragraph 1).

In response, the Examiner notes that the claim does not define what a "predefined timing relationship" is. Absent further claim limitations defining the relationship between the signals and CLK, any relationship between the signals is a predefined relationship within the scope of the claims.

40. Applicant has argued that Honma does not teach a predetermined timing relationship between the no address signal and a first clock edge (See Page 16 Paragraph 2). In response, the Examiner notes that the claim does not define what a "predefined timing relationship" is. Absent further claim limitations defining the relationship between the no address signal and a clock signal, any relationship between the signals is a predefined relationship within the scope of the claims.

41. Applicant has argued that McIntyre does not teach a predetermined timing relationship between the early burst request signal and a first clock edge (See Page 17 Paragraph 1). In response, the Examiner notes that the claim does not define what a "predefined timing relationship" is. Absent further claim limitations defining the relationship between the early burst request signal and a clock signal, any relationship between the signals is a predefined relationship within the scope of the claims.

42. Applicant has argued that Ohuchi and McIntyre do not present signal a burst request signal a delay after a first clock signal (See Page 17 Paragraph 2). In response, the Examiner notes that the claim does not define what the delay is.

Because there is inherently a delay in the control logic of McIntyre (See Figure 1 Number 4), the burst request signal is presented a delay after the first clock signal.

43. Applicant has argued that Hirose does not teach request and grant signals being received and presented at a master interface to a bus (See Page 18 Paragraph 1). In response, the Examiner notes that Hirose is being relied upon to teach a device receiving a bus request signal and generating a bus grant signal, and Ohuchi is being relied upon to teach receiving and presenting signals at a master interface.

44. Applicant has argued that Hirose does not teach presenting the command signal at the slave interface (See Page 18 Paragraph 2). In response, the Examiner notes that the control logic is part of the slave interface, and as such, the command signal generated by the control logic is presented to the slave interface.

45. Applicant has argued that Pincus does not teach the master interface receiving a lock signal (See Page 19 Paragraph 1). In response, the Examiner notes that the claim does not require the signal to be received from the bus and does not prohibit the signal being received from elsewhere, including from the master device connected to the master interface, which then sends the received lock signal to the control logic.

46. Applicant has argued that Picazo does not teach a second multiplexer configured to select a write data select signal responsive to a bus grant signal. In response, the

Examiner notes that element 610 is bus grant logic and not a multiplexer. Picazo teaches that the control logic comprises a first multiplexer configured to multiplex control signals, which are equivalent to the early signals, responsive to the bus grant signal (See Figure 6B Numbers 610, 632, 604, 608, 660, 622, and 637 and Column 31 Lines 32-36). Picazo further teaches a second multiplexer that selects a write control signal based on the bus grant signal (See Figure 6B Numbers 610 and 640 and Column 31 Lines 25-31).

Conclusion

47. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Thomas J. Cleary whose telephone number is 571-272-

3624. The Examiner can normally be reached on Monday-Thursday (7-3:30), Alt. Fridays (7-2:30).

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Mark H. Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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